AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A disk array apparatus comprising:

a cache memory that temporarily stores data to be read from or written to ~~first and second~~ disks; and

a control unit which generates a check information on the basis of said data, transforms said data ~~and said check information~~ into a physical domain of said cache memory so as to associate said data ~~and said check information~~ with physical addresses, thereafter stores data to be newly written corresponding to said physical addresses in a logical domain of said cache memory and ~~processes preferentially for writing the~~ take precedence writing said data and check information over writing said data to be newly written ~~associated with the physical addresses in the cache memory to the first and second disks,~~

~~wherein said control unit processes substantially simultaneously said data and said check information to said first and second disks~~.

2. (original) The disk array apparatus as claimed in

claim 1, wherein said control unit releases the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed.

3. (original) The disk array apparatus as claimed in claim 1, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein if a failure occurs in one control unit, another control unit takes over the preferential processing for the data associated with a physical address in the cache memory.

4. (original) The disk array apparatus as claimed in claim 1, wherein said cache memory is a nonvolatile memory.

5. (original) The disk array apparatus as claimed in claim 2, wherein said cache memory is a nonvolatile memory.

6. (original) The disk array apparatus as claimed in claim 3, wherein said cache memory is a nonvolatile memory.

7. (currently amended) A data writing method in a disk array apparatus for reading and writing data from and to a plurality of disks in accordance with a command issued from an upper-level host computer, the method comprising:

before executing a processing for writing data to the plurality of disks, storing data associated with logical addresses in a logical domain of a cache memory;

generating a check information on the basis of said data;

transforming said data ~~and said check information~~ to a physical domain of said cache memory so as to associate said data ~~and said check information~~ with physical addresses;

thereafter storing data to be newly written corresponding to said physical addresses in a logical domain of said cache memory; and

taking precedence writing said data and check information over writing said data to be newly written ~~and~~

~~substantially simultaneously writing the data and said check information from the physical domain of the cache memory to first and second ones of the plurality of disks to maintain data coherency~~.

8. (previously presented) The data writing method as claimed in claim 7, further comprising:

releasing the data associated with the physical addresses in the cache memory from a state in which the data is associated with the physical addresses after confirming that the writing is completed.

9. (original) The data writing method as claimed in claim 7, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein, if a failure occurs in one control unit, another control unit takes over the preference processing for the data associated with a physical address in the cache memory.

10. (original) The data writing method as claimed in claim 8, wherein said control unit comprises a plurality of control units which are physically independent of one another and wherein, if a failure occurs in one control unit, another control unit takes over the preference processing for the data associated with a physical address in the cache memory.

11-16 (cancelled).